UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,005	06/15/2001	Shuo-Yen Robert Li	Li 17	9906

570 7590 10/04/2005

AKIN GUMP STRAUSS HAUER & FELD L.L.P.
ONE COMMERCE SQUARE
2005 MARKET STREET, SUITE 2200
PHILADELPHIA, PA 19103

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,005	LI, SHUO-YEN ROBERT	
	Examiner	Art Unit	
	Ian N. Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-27 and 29-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-40* is/are allowed.

6)☒ Claim(s) *17-27,29-35,41 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. **The previous objections to drawings are hereby incorporated**. The drawings are objected to because reference numbers in FIG. 6B-F, 7,9,10,12-19,44A-C, 69, and 71A-B because they lack the descriptive legends or labels.

The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Yang (U.S. 5,987,028).

Regarding Claim 17, Yang discloses a method for self-routing a packet (see col. 10, lines 1-30; self-routing the cell) to a given destination address (see FIG. 11 and 20, output address $d_{n-1}\, d_{n-2} \ldots d_0$; see col. 10, lines 9-14) through a bit-permuting network (see FIG. 5, 8, 9, 11 or 20; a bene, batcher, or banyan network) having 2^n input ports and 2^n output ports (see FIG. 5, 8, 9, 11 or 20; input and output ports), the network being characterized by a guide (see col. 10, lines 5-9; a control sequence: $c_{m-1}\, c_{m-2} \ldots c_0$), the method comprising:

generating a routing tag (see FIG. 10, lines 10-14; see col. 17, lines 54 to col. 18, lines 14; routing tag R) for the packet based on the guide of the network and the destination address (see col. 10, lines 9-14; create a routing tag based upon control sequence and an output/destination address), and

routing the packet through the network using the routing tag (see col. 10, lines 1-54; see col. 17, lines 54 to col. 18, lines 14).

4. Claims 17-20,22-26,30-32 and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. 6,335,930).

Regarding Claim 17, Lee discloses a method for self-routing a packet (see col. 9, lines 60-65; see col. 10, lines 1-9; self-routing the packet) to a given destination address (see FIG. 2, 6 and 7, destination/output address; see col. 4, lines 9-25; see col. 10, lines 15-25) through a bit-permuting network (see FIG. 6 and 7; NxN network 600 and 700) having 2^n input ports and 2^n output ports (see FIG. 6 and 7; input ports 601 and output ports 602) the network being characterized by a guide (see FIG. 7, the routing bit; see col. 10, lines 5-9), the method comprising:

generating a routing tag (see FIG. 8, a routing tag; see col. 9, lines 65-67) for the packet based on the guide of the network and the destination address (see col. 10, lines 1-49; creating a routing tag based on the routing bit and destination address), and

routing the packet through the network using the routing tag (see col. 10, lines 9 to col. 11, lines 55; routing in accordance with a routing tag).

Regarding Claim 18, Lee discloses wherein the network is a k-stage network (see FIG. 6-7, STG601-STG604, where k=4 stages network) composed of nodes (see FIG. 6-7, switching elements; see col. 8, lines 40-50) and the destination address is expressed as binary ($d_1d_2 \ldots d_k$) (see FIG. 6-7, binary output address 111 or 110; see col. 10, lines 15-67) and the guide is expressed as (1), γ (2), . . . , γ(k) (see FIG. 7, the routing bit; see col. 10, lines 5-9) where γ is a mapping from the set [1, 2, . . . , k] (see FIG. 6-7, k=4 stages) to the set [1, 2, . . . , n] (see FIG. 6-7, 601-1 to 601-8, n=8), and wherein the generating a routing tag includes generating binary (see FIG. 8, a routing tag; see col. 9, lines 65-67; see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address).

Regarding Claim 19, Lee discloses prepending binary ($d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$) to the packet (see FIG. 8, see col. 15, lines 50-60; col. 10, lines 1-49; a routing tag is appended/attached to the packet).

Regarding Claim 20, Lee discloses for a j-th stage node, the routing includes using $d_{\gamma(j)}$ in the j-th stage node to select an output from the j-th stage node to emit the packet, (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4; see FIG. 7, see col. 10, lines 15 to col. 11, lines 55; see col. 17, lines 28-54).

Regarding Claim 22, Lee discloses a method for self-routing a packet (see col. 9, lines 60-65; see col. 10, lines 1-9; self-routing the packet) through a 2^n x 2^n switch (see FIG. 6 and 7; NxN switch 600 or 700), the switch having 2^n external output ports labeled with 2^n distinct binary output addresses in the form of $b_1b_2 \ldots b_n$, (see FIG. 6 and 7, output ports with binary output address 00,01,10, 11; see col. 8, lines 58 to col. 9, lines 30; see col. 10, lines 9-14) and comprising a plurality of switching cells (see FIG. 6-7, switching elements; see col. 8, lines 40-

50) and interconnected into a k-stage bit-permuting network (see FIG. 6-7, STG601-STG604, where k=4 stages network) which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9) where γ is a mapping from the set [1, 2, . . ., k] (see FIG. 6-7, k=4 stages) to the set [1, 2, . . ., n] (see FIG. 6-7, 601-1 to 601-8, n=8), wherein each of the switching cells is a sorting cell associated with the partial order "0 (`0-bound`)1 (`1-bound`)" (see FIG. 6-7, 00,01,10 and 11 switching elements in STG600; see col. 8, lines 58-65), the packet being destined for a binary output address $d_1d_2 \ldots d_n$ (see FIG. 6-7, binary output address 111 or 110; see col. 10, lines 15-67) the method comprising:

generating a routing tag $d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(k)}$ (see FIG. 8, a routing tag; see col. 9, lines 65-67; see col. 15, lines 50-60) for the packet based on the guide and the destination output address of the packet (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address), and

routing the packet through the network by using $d_{\gamma(j)}$ in the routing tag in the j-th stage cell, $1 \leq j \leq k$, (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55; see col. 17, lines 28-54).

Regarding Claim 23, Lee discloses wherein the routing includes removing the bit $d_{\gamma(j)}$ from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at switching element 704-2 (i.e. 0<u>11</u>) before sending the packet; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 24, Lee discloses wherein the routing includes using the leading bit from the routing tag in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-th stage cell to

emit the packet(see FIG. 2,6, and 7; packet A with routing tag 111, using the first bit at 704-2 (i.e. 011) before sending the packet to select the output; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 25, Lee discloses wherein the routing includes removing the leading one bit from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bit of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $d_{\gamma(j)}$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at 704-2 (i.e. 011) before sending the packet such that "1" from the roting tag 111 in the stage 704-2 is 011; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 26, Lee discloses wherein the routing includes rotating the leading one bit of the routing tag of the packet to the end of the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bit of the routing tag in the j-the stage cell, $1 \leq j \leq k$, is always $d_{\gamma(j)}$ (see FIG. 2; see col. 3, lines 60 to col. 4, lines 25; rotating first bit "0" at 001 to 010 at STG201, or rotating first bit "0" at 010 to 100 at STG202; also see FIG. 6-7)

Regarding Claim 30, Lee discloses wherein generating the routing tag includes generating the routing tag $1d_{\gamma(1)}d_{\gamma(2)}\ldots d_{\gamma(k)}$ (see FIG. 8, a routing tag; see col. 9, lines 65-67; and see col. 10, lines 15 to col. 11, lines 60; routing tag which begins with 1, i.e. 111,101, and etc.) for a real data packet (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address for real/actual data).

Regarding Claim 31, Lee discloses the routing includes using $1d_{\gamma(k)}$ in the routing tag of the real data packet in the j-th stage cell, $1 \leq j \leq k$, (see FIG. 7, STG702 or STG703, where j=2 or 3

which is less than k=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55; see col. 17, lines 28-54).

Regarding Claim 32, Lee discloses wherein the routing includes removing the bit $d_{\gamma(j)}$ from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at 704-2 (i.e. 0<u>11</u>) before sending the packet; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Regarding Claim 41, Lee discloses a 2^n x 2^n self-routing switch (see FIG. 6 and 7; self routing NxN switch 600 or 700; see col. 9, lines 60-65; see col. 10, lines 1-9) having an array of 2^n external input ports (see FIG. 6-7, binary input ports/address; 00,01,10,11) and an array of 2^n external output ports with 2^n distinct binary output addresses in the form of $b_1b_2 \ldots b_n$ for switching a packet (see FIG. 6 and 7, output ports with binary output address 00,01,10, 11; see col. 8, lines 58 to col. 9, lines 30; see col. 10, lines 9-14), the packet being either a real data packet destined for an n-bit binary destination address, or being an idle packet having no pre-determined destination output address (see col. 15, lines 55 to col. 16, lines 40; active/real or idle packet), the switch comprising:

a switch fabric (see FIG. 6-7, a combined system of STG601-STG604 or STG701-STG704) with external input ports (see FIG. 6, input ports 601), the switch fabric having a plurality of switching cells (see FIG. 6, 603-1 to 603-4, 604-1 to 604-4,..) interconnected into a k-stage bit-permuting network (see FIG. 6-7, STG601-STG604, where k=4 stages network) which is characterized by the guide $\gamma(1), \gamma(2), \ldots, \gamma(k)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9), where γ is a mapping from the set $[1, 2, \ldots, k]$ (see FIG. 6-7, k=4 stages) to the set $[1, 2, \ldots, n]$ (see FIG. 6-7, 601-1 to 601-8, n=8),

a routing tag circuit, coupled to the external input ports (see FIG. 8, a routing tags are created at the input; see col. 9, lines 65-67), for generating a routing tag $1d_1d_2\ldots d_n$ (see FIG. 8, a routing tag; see col. 9, lines 65-67; and see col. 10, lines 15 to col. 11, lines 60; routing tag which begins with 1, i.e. 111,101, and etc.) for each of the real data packets based on the guide of the bit-permuting network and the destination output address of the packet (see col. 10, lines 1-49; creating a routing tag with reference to the routing bit and destination address for real/actual data), and

a routing control circuit, coupled to the switching cells (see FIG. 15 and 19, input port controller 1502; see col. 16, lines 44-65; see col. 19, lines 60 to col. 20, lines 10), for routing the real data packet through the switch by using $1d_{\gamma(j)}$ in the routing tag of the packet in the j-th stage cell, $1 \leq j \leq k$ (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than k=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 21 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Song (U.S. 5,963,554)

Regarding Claim 21, Lee discloses wherein the network is an n-stage network (see FIG. 6, Nx N network), the guide is expressed as $\gamma(1), \gamma(2), \ldots, \gamma(n)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9), where γ is a permutation on the integers from 1 to n and wherein, for a j-th stage node (see FIG. 7, STG702 or STG70, wherein $j \leq n$), the routing includes using in the j-th stage node to select an output from the j-th stage node to emit the packet, $1 \leq j \leq n$ (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than n=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55).

Lee does not explicitly disclose banyan type network. However, Song teaches a banyan type network (see FIG. 3, see col. 5, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a banyan type network, as taught by Song in the system of Lee, so that it would provide an effective and improved switching device; see Song col. 1, line 64 to col. 2, lines 49.

Regarding Claim 27, wherein the network is an n-stage network (see FIG. 6, Nx N network), the guide is expressed as $\gamma(1), \gamma(2), \ldots, \gamma(n)$ (see FIG. 7, the routing bit; see col. 10, lines 5-9), where γ is a permutation on the integers from 1 to n and wherein the generating a routing tag includes generating tag $d_{\gamma(1)} d_{\gamma(2)} \ldots d_{\gamma(n)}$ (see FIG. 7, STG702 or STG703, where j=2 or 3 which is less than n=4), to select an output from the j-th stage cell to emit the packet (see FIG. 7, see col. 10, lines 15 to col. 11, lines 55).

Lee does not explicitly disclose banyan type network. However, Song teaches a banyan type network (see FIG. 3, see col. 5, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize a banyan type

network, as taught by Song in the system of Lee, so that it would provide an effective and improved switching device; see Song col. 1, line 64 to col. 2, lines 49.

7. Claim 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Kerstein (U.S. 6,058,112).

Regarding Claim 29, Lee discloses wherein the sorting cell is associated with the partial order "10 (0-bound), 00 (bound), 11 (1-bound)" (see FIG. 6 and 7; STG601 with "10" (for element 603-3), "00" (for element 603-1), and "11" (for element 603-4); see col. 8, lines 58-65. Yang also discloses idle packet

Lee does not explicitly disclose "00 (idle)". However, Kerstein teaches "00 (idle)" (see col. 6, lines 43-46; "00" indicates that the data is idle bound). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "00" for an idle data, as taught by Kerstein in the system of Lee, so that it would diagnosed to determine if the switch is working properly, and monitored while it is operating to verify its operation; see Kerstein col. 1, line 34-67 and col. 6, lines 30-67.

8. Claims 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Yang (U.S. 5,987,028).

Regarding Claim 33, Lee discloses wherein the routing includes using the leading one bit from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-the stage cell to emit the packet (see FIG. 2,6, and 7; packet A with routing tag 111, using

the first bit at 704-2 (i.e. 0<u>11</u>) before sending the packet to select the output; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4).

Lee does not explicitly disclose leading two bits. However, Yang teaches using the leading two bits of the routing tag (see FIG. 11, (c) <u>10</u> 101, first two bits "10", c1c0) in the j-th stage cell, $1 \leq j \leq k$, to select an output from the j-the stage cell to emit the packet (see col. 10, lines 34-37; see col. 17, lines 54 to col. 18, lines 14). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide leading two bits for routing, as taught by Yang in the system of Yang, so that it would overcome the disadvantages of the prior art by providing the method of assigning routing tag bits for routing signals; see Yang col. 5, line 15 to col. 9, lines 21.

Regarding Claim 34, Lee discloses wherein the routing includes removing the leading one bit from the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ (see FIG. 2,6, and 7; packet A with routing tag 111, removing the first bit at 704-2 (i.e. 0<u>11</u>) before sending the packet such that "1" from the routing tag 111 in the stage 704-2 is 0<u>11</u>; see col. 3, lines 60 to col. 4, lines 25; see col. 10, lines 15 to col. 11, lines 4). Yang discloses leading two bits in routing tag, $1 \leq j \leq k$, such that two leading bits of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ as described above in claim 33. Thus, the combined system of Lee and Yang discloses removing the second leading one bit of the two leading bits from the routing tag for routing. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide leading two bits for routing, as taught by Yang in the system of Yang, for the same motivation as described above in claim 33.

Regarding Claim 35, Lee discloses wherein the routing includes rotating the leading one bit of the routing tag of the packet to the end of the routing tag before the packet exists the j-th stage cell, $1 \leq j \leq k$, such that the leading bits of the routing tag in the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ (see FIG. 2; see col. 3, lines 60 to col. 4, lines 25; rotating first bit "0" at $\underline{0}01$ to $01\underline{0}$ at STG201, or rotating first bit "0" at $\underline{0}10$ to $10\underline{0}$ at STG202; also see FIG. 6-7). Yang discloses leading two bits in routing tag, $1 \leq j \leq k$, such that two leading bits of the routing tag is the j-the stage cell, $1 \leq j \leq k$, is always $1d_{\gamma(j)}$ as described above in claim 33. Thus, the combined system of Lee and Yang discloses removing the second leading one bit from the routing tag for routing. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide leading two bits for routing, as taught by Yang in the system of Yang, for the same motivation as described above in claim 33.

9. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Newman (U.S. 5,367,518).

Regarding Claim 42, Lee discloses wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, (see col. 13, lines 35-60; col. 16, lines 60-65; col. 17, lines 50-65; see FIG. 8, routed number; different priorities for different routing numbers are assigned/classified), and wherein the routing tag circuit includes a generator for generating a routing tag (see FIG. 8, a routing tags are created/generated at the input; see col. 9, lines 65-67), for each of the real data packets of the form $d_{\gamma(1)} \ldots d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag (see FIG. 8, a routing tag; see col. 9, lines 65-67; see col. 15, lines 50-60).

Lee does not explicitly disclose wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$ and $d_{\gamma(1)} p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$. However, Newman teaches wherein the real data packets are classified into 2^r priority classes, $r \geq 1$, (see FIG. 9, Priority Unit 46 with classes 46-0 to 46-(N-1)) wherein each of the priority classes is coded in an r-bit string $p_1 \ldots p_r$, (see col. 15, lines 45 to col. 16, lines 15-68; bits in the priority tag) and wherein the routing tag circuit includes a generator (see FIG. 1, Input controller 6) for generating a routing tag for each of the real data packets of the form $d_{\gamma(1)} p_1 \ldots p_r d_{\gamma(2)} \ldots d_{\gamma(k)}$ as the routing tag (see col. 5, lines 57 to col. 6, lines 14; a routing tag and priority tags are created and added to the incoming packets). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide coded priority classes and a tag bit form which consists both routing and priority tags, as taught by Newman in the system of Lee, so that it would provide an improved switching system by utilizing priority tags associated with the routing tag to determine among competing inputs which one or ones will be transmitted through the packet switch; see Newman col. 3, line 40 to col. 4, lines 45.

Allowable Subject Matter

10. Claims 36-40 are allowed.

Response to Arguments

11. Applicant's arguments filed 7/7/2005 have been fully considered but they are not persuasive.

Applicant traverses the previous objections to **the drawings** by citing 37 § C.F.R 1.83 that there are such no requirement in MPEP to do so (see remarks page 9, paragraph 3-6).

In response to the applicant arguments, applicant attention is directed to **MPEP § 608.02(e) Examiner Determines Completeness and Consistency of Drawings**. Thus, it is clear in accordance with MPEP which states that the "examiner", <**NOT the applicant< ,** determines the completeness and consistency of drawings [emphasize added]. In this case, examiner has determined that the drawings are **incomplete**.

The applicant attention is also directed to **37 § C.F.R 1.84 [5(o)]** which states "**Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.**" In this case, examiner is clearly requiring the applicant to include "suitable descriptive legends" that is necessary for the understanding for the drawings since the drawings are **incomplete**.

Moreover, the examiner is requiring this application to be in the best presentable and complete form for the public including patent community, who will appreciate the completeness of this application once published or issued. Examiner wonders why the applicant is arguing or traversing the drawing objections since by traversing the objection will remain the application in an incomplete or un-presentable form.

Therefore, the objections to the drawings stand objected as set forth previous and above. The objection to the drawings will not be held in abeyance.

Regarding claims 17-20, the applicant argued that, "...$(\sigma_1 \sigma_2 \ldots \sigma_{k-1})$ (n), $(\sigma_2 \ldots \sigma_{k-1})$ (n),..., $(\sigma_{k-2} \sigma_{k-1})$ (n), σ_{k-1} (n),n,...k is the number of stages in the networks, σ_k is the

permutation between k01 stage and k stage of the network", "the state of each cell...at which the packet is received" in page 11, second last paragraph; page 12, paragraph 1; page 13, paragraph 3,5.

Regarding claim 17, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "...($\sigma_1\ \sigma_2 \ldots \sigma_{k-1}$) (n), ($\sigma_2 \ldots \sigma_{k-1}$) (n),..., ($\sigma_{k-2}\ \sigma_{k-1}$) (n), σ_{k-1} (n),n,...k is the number of stages in the networks, σ_k is the permutation between k01 stage and k stage of the network", "the state of each cell...at which the packet is received") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding claim 17, the applicant argued that, "...the claimed method of construction a routing tag is different from the method disclosed by Yang...Yang is specific to a Benes type network...the method of amended claim 17 is applicable to **any** bit-permuting network **including not limited** to Banyan type network, baseline networks, Omega networks and divide and conquer networks..." in page 12, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees the argument above. Yang discloses generating a routing tag **(see FIG. 10, lines 10-14; see col. 17, lines 54 to col. 18, lines 14; routing tag R)** for the packet based on the guide of the network **(see col. 10, lines 5-9; a control sequence: $c_{m-1}\ c_{m-2} \ldots c_0$)** and the destination address **(see FIG. 11 and 20, output address $d_{n-1}\ d_{n-2} \ldots d_0$; see col. 10, lines 9-14: see col. 10, lines 9-14; create a**

routing tag based upon control sequence and an output/destination address). Thus, examiner finds no <u>different</u> between claimed method and Yang's method.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **Banyan type network, baseline networks, Omega networks and divide and conquer networks**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). **Even if they are recited in the claim**, Yang still teaches a bit-permutation networks a bene, batcher, or banyan network as disclosed in FIG. 5, 8, 9, 11 or 20. Note that the claimed limitation "bit-permuting network", <u>as admitted by the applicant</u>, is "<u>**any**</u> bit-permuting network". Therefore, **any** bit permuting network will read on the applicant claimed network. In this case, Yang's bit-permuting networks' bene, batcher, and/or banyan networks <u>clearly</u> read on the applicant claimed network. Moreover, since the applicant states "**any** bit-permuting network **including not limited** to Banyan type network, baseline networks, Omega networks and divide and conquer networks", it is clear that the <u>applicant is admitting</u> that Yang's bene, batcher, or banyan network are "a bit-permuting" networks.

Regarding claim 17, the applicant argued that, "...in order to be considered a bit-permuting network (1) the switching elements must be 2x2 switches; (2) every stage of the network must consists of 2^{n-1} 2x2 switches, and (3) every exchange in the network must be bit-permuting...the switching elements disclosed by Lee are <u>not</u> 2x2 switching elements..." in page 13, paragraph 1.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **(1) the switching elements must be 2x2 switches; (2) every stage of the network must consists of 2^{n-1} 2x2 switches, and (3) every exchange in the network must be bit-permuting**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Lee discloses 2x2 network (in FIG. 6 and 7 NxN network 600 and 700), where N=2. having 2^n input ports and 2^n output ports (see FIG. 6 and 7; input ports 601 and output ports 602, where input/output port, $2^n = 2^{n=0} = 2^0 = 1$ (i.e. 1 port), $2^n = 2^{n=1} = 2^1 = 2$ (i.e. 2 ports), etc. Thus, in view of simple mathematical illustration, it is clear that applicant claimed invention is **not limited** to **2x2** as applicant is arguing since the variable N can be 0,1, 2,...n, and both input/output port can be 1 to n. Thus, it is clear that Lee discloses the argued limitations.

Regarding claims 17, 22, 21,27, 29, 33-35, 41 and 42, the applicant argued that, "...Lee does not teach or suggest generation a routing tag based on a guide..." in page 13, paragraph 4; page 14, paragraph 1; page 14, paragraph 4; page 15, paragraph 4-5; page 16, paragraph 1,4; page 17, paragraph 2

In response to applicant's argument, the examiner respectfully disagrees the argument above. Lee discloses generation a routing tag (**see FIG. 8, a routing tag; see col. 9, lines 65-67**) based on a guide (**see FIG. 7, the routing bit; see col. 10, lines 5-9**) and the destination address (**see FIG. 2, 6 and 7, destination/output address; see col. 4, lines 9-25; see**

col. 10, lines 15-25; see col. 10, lines 1-49; creating a routing tag based on the routing bit and destination address).

Regarding claims 22, 29, 41 and 42, the applicant argued that, "...Lee teaches a bypass Omega network. A bypass Omega network is not a bit permuting network because each of the switching is not 2x2 switch…" in page 13, paragraph 4; page 14, paragraph 4; page 16, paragraph 1; page 17, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees the argument above. Lee discloses a bit permuting network (see FIG. 6 and 7; NxN network 600 and 700 utilizes bit permuting "000" to "111"). Lee discloses a 2x2 switch as stated in above response.

Regarding claims 22, 27 and 33-35, the applicant argued that, "...a sorting cell is a 2x2 switching element …where 0<1 has a truth table of: connection state…" in page 14, paragraph 1; page 15, paragraph 5; page 16, paragraph 4.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **a sorting cell is a 2x2 switching element …where 0<1 has a truth table of: connection state**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
INM
9/29/05

Chau T. Nguyen

CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600